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# DESIGN AND IMPLEMENTATION OF A KA-BAND SILICON-BASED 3D-HETEROGENEOUS-INTEGRATED 8-CHANNEL TRANSMIT MICROSYSTEM

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**Abstract:** This paper presents the design and implementaion of a Ka-band Silicon-Based 3D-Heterogeneous-Integrated 8-channel transmit microsystem. By introducing capacitive and inductive transition structures in the 3D passive interconnections of the microsystem, up to 40GHz broadband impedance matching is realized. Meanwhile, a three-layer Cu-Sn bonded silicon interposer architecture and its corresponding fabrication process are developed for the implementation of the two stacked sub-modules. And sub-modules stacking and fan-out of ball grid array (BGA) pins are achieved using solders and solder balls with differentiated temperature gradients. The fabricated 8-channel transmit microsystem features 1 input port and 8 output ports, with an operating frequency band over 27–32 GHz, a saturated output power of 23 dBm, an overall dimensions of 9.1 mm × 8.5 mm × 3.25 mm, and a weight of less than 0.1 g per channel.

**Keywords:** 3D heterogeneous integration; Microsystem; Silicon interposer; Metal bonding; Temperature gradient

## 1 INTRODUCTION

With the ever-increasing demands for high functional density, superior performance and high operating frequency in phased array radars, achieving the key radio frequency (RF) performance of each channel within the limited physical dimension corresponding to antenna element spacing has emerged as a critical technical challenge [1-2]. Over the past two decades, the integration scheme of TR modules has evolved from board-level integration with single-chip packaging to multi-chip module (MCM) and system-in-package (SiP) integration [3-5]. However, multi-chip packaging technologies based on ceramic substrates or printed circuit boards (PCBs) only enable high-density integration in the planar dimension. In addition, constrained by manufacturing process capabilities, the characteristic dimensions of transmission lines often reach tens or even hundreds of micrometers. As the operating frequency of phased array radars moves toward the millimeter-wave band, the antenna element spacing is continuously reduced, rendering traditional planar multi-chip packaging technologies incapable of meeting practical application requirements. To fully exploit the vertical spatial dimension, researchers have proposed package-on-package (PoP) technology [6]. In recent years, to further enhance the RF performance of PoP architectures, PoP packaging solutions based on organic substrates, silicon interposers and glass substrates have been successively developed for phased array applications. Among these solutions, silicon interposer-based PoP packaging is the most widely adopted in TR modules and is also recognized as a key branch of 3D heterogeneous integration (3D-HI) microsystems.

Compared with organic substrates, silicon interposers exhibit higher material stability, which confers distinct advantages in hermetic packaging and long-term operational reliability. In comparison with glass substrates, silicon interposers benefit from mature semiconductor manufacturing processes and excellent thermal dissipation performance. Owing to these characteristics, organic substrate-based PoP is commonly used for packaging high-density input/output (IO) chips (e.g., field-programmable gate arrays, FPGAs), while glass substrate-based PoP is suitable for low-power or passive devices (e.g., antennas, filters). By contrast, silicon interposer-based PoP, or silicon-based 3D heterogeneous microsystems, has become a pivotal development direction for the next-generation phased array TR modules [7-9].

Silicon-based 3D heterogeneous microsystem technology enables the decomposition of an entire functional circuit into multiple modular subunits, which are then vertically integrated via through-silicon vias (TSVs) and wafer-level bonding [10-12]. In recent years, microsystem architectures based on this concept have been continuously refined. For instance, Yan et al. and Zhao et al. mounted chips on the surface of silicon interposers using flip chip (FC-BGA) bonding and wire bonding techniques [13-14]; Ming et al. integrated integrated passive devices (IPDs) on silicon interposers to realize a 2.5D architecture [15]; Yoon et al.

proposed a module stacking approach via reflow soldering for 3D architecture implementation [16-17]; and Zhong et al. achieved hermetic packaging of silicon interposers through eutectic bonding [18]. Despite its broad application prospects, silicon-based 3D heterogeneous microsystem technology still faces several unresolved technical challenges. For example, conventional hermetic packaging relies on Au-Sn or Au-Au material systems [19-21], which require processing at high temperatures (300 °C–350 °C) and a gold layer thickness of more than 6 µm. These stringent parameter requirements not only degrade chip performance but also result in exorbitant packaging process costs.

To address the aforementioned issues associated with metal systems in hermetic packaging, this paper proposes a microsystem architecture based on silicon-based 3D heterogeneous integration technology. By introducion capacitive and inductive transition structures in the 3D passive interconnections of the microsystem, up to 40GHz broadband impedance matching is realized. By adopting a pre-tinned bonding metal layer technology and utilizing a Cu-Sn metal system, the high-temperature bottleneck inherent in Au-Sn or Au-Au systems is effectively circumvented. Meanwhile, solders and solder balls with differentiated temperature gradients are employed to realize sub-module stacking and BGA pin fan-out. Based on the proposed technologies, a Ka-band 8-channel transmit module is fabricated, and its morphological characterization and electrical performance testing are conducted in this work.

## 2 MICROSYSTEM DESIGN

For phased array antennas, when the operating frequency is elevated to the Ka band and above, TR modules based on planar integration can no longer satisfy the dimensional constraints imposed by antenna element spacing. Thus, utilizing the vertical spatial dimension through module stacking has become an inevitable development trend for TR modules. We designed an 8-channel transmit microsystem (as illustrated in Figure 1) implemented by a hybrid scheme integrating one silicon-based 8-channel amplitude-phase multifunctional chip and four dual-channel compound power amplifier chips, with an operating frequency band of 27–32 GHz and a saturated output power of 23 dBm.

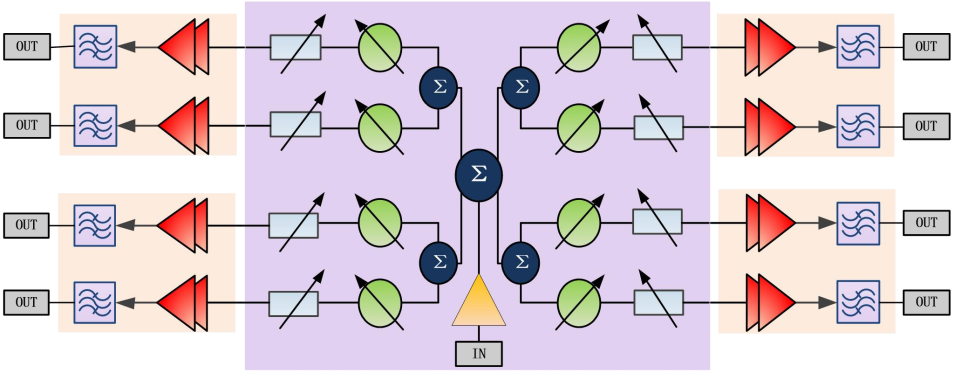


**Figure 1** Block Diagram of the Microsystem Link

### 2.1 Link Budget and RF Cascade Simulation

The RF signal transmission path is as follows: the RF signal is fed into the microsystem through the common (COM) port, undergoes phase and amplitude adjustment by the amplitude-phase multifunctional chip (MF), and is then routed to the power amplifier (PA). After signal amplification and filtering, the signal is output through each antenna port. The RF signal propagates through various transmission line (TL) structures within the microsystem, including microstrip lines, coplanar waveguides with ground (CPWG), and coaxial-like structures, all of which are taken into account in the link budget analysis. The link budget of the transmit channel is summarized in Table 1.

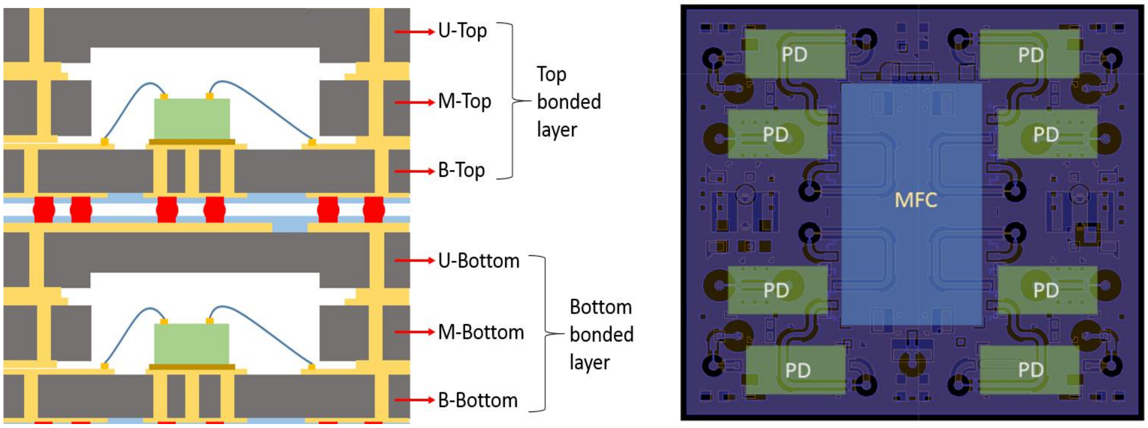
**Table 1** Link Budget of the Transmission Channel

| Microsystem/Structure | Gain (dB) | Cumulative Gain (dB) | Input Power (dBm) | Output Power (dBm) |
|---|---|---|---|---|
| Transition | -0.5 | -0.5 | -1 | -1.5 |
| Amplitude-phase multifunctional chip | 1 | 0.5 | -1.5 | -0.5 |
| Power amplifier & | 25 | 25.5 | -0.5 | 24.5 |

| | | | | |
|---|---|---|---|---|
| filtering | | | | |
| Transition | -0.5 | 25 | 24.5 | 24 |

### 2.2 Simulation and Layout Design

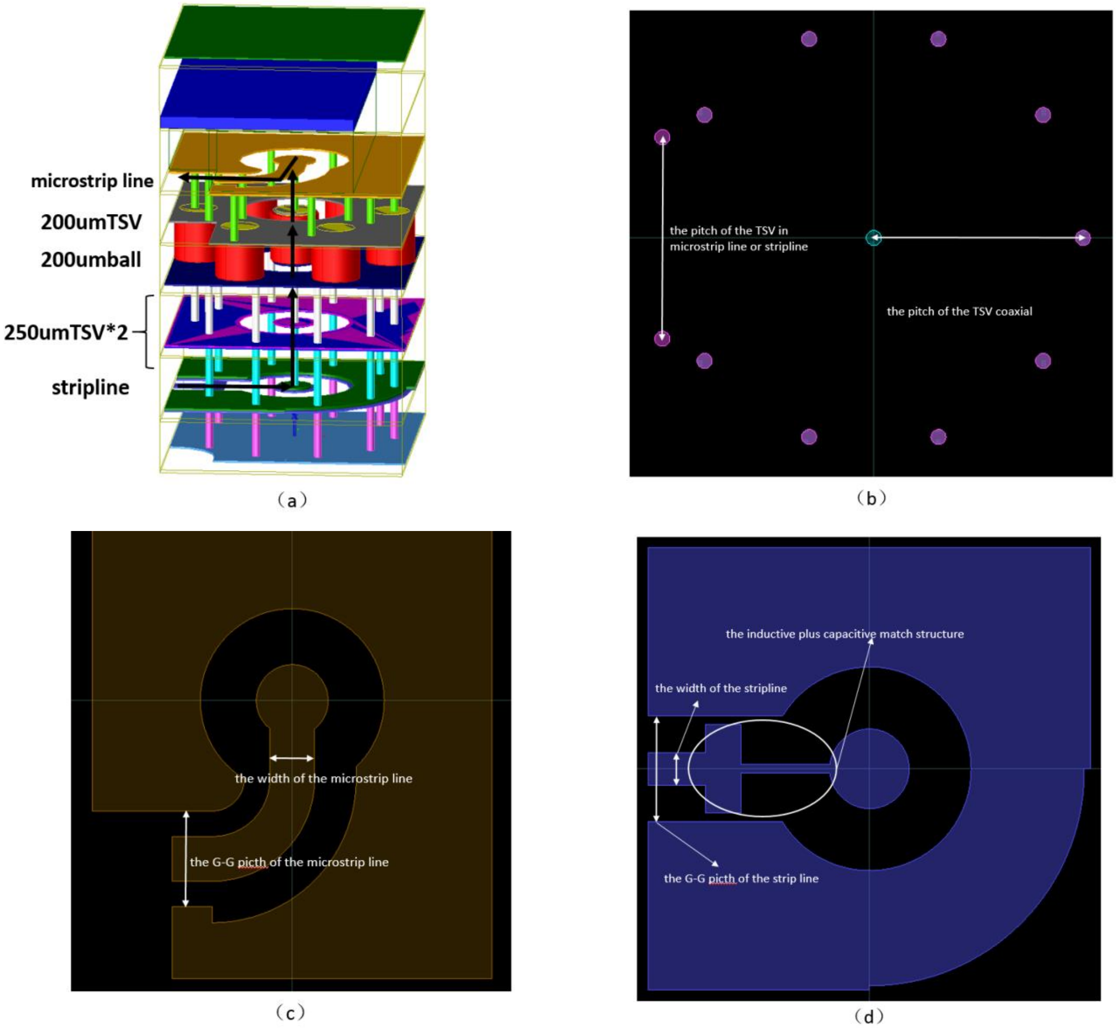
In this transmit microsystem, six silicon wafers are utilized to realize double-layer chip stacking. Each chip layer is packaged by a bottom interposer (denoted as B, with a thickness of 200 μm), a middle interposer (denoted as M, with a thickness of 250 μm), and an upper interposer (denoted as U, with a thickness of 250 μm), which are then vertically stacked to form a 3D heterogeneous microsystem (as shown in Figure 2(a)). The overall layout of the two chip layers is presented in Figure 2(b), where equal-length routing is adopted for the RF traces of all channels to ensure phase consistency.



(a) (b)

**Figure 2** (a) Cross-Section of the Two-Layer Microsystem; (b) Chip Layout

As mentioned previously, the microsystem incorporates a variety of TL structures that constitute the RF signal transmission paths and play a decisive role in determining the RF performance of the microsystem. A typical TL structure is elaborated in detail below. In the designed microsystem, a typical TL structure consists of striplines, microstrip lines, TSVs, and BGA coaxial-like structures (as depicted in Figure 3(a)). Figure 3(b) shows the TSV coaxial-like structure, where the ground-signal (G-S) spacing between the signal TSV and the ground TSV is 346 μm. The spacing of the left TSV is adjusted to 400 μm to avoid the transition structure of microstrip lines and striplines. Impedance mismatch is inevitable at the interface between the TSV coaxial-like structure and the transition structure. To mitigate this issue, a matching structure is designed by introducing equivalent inductance and capacitance to suppress impedance discontinuities (as shown in Figure 3(c) and 3(d)). The microstrip line has a width of 112 μm, with a ground-ground (G-G) spacing of 240 μm for the ground patterns on both sides. The stripline features a width of 74 μm and a G-G spacing of 240 μm for the lateral ground patterns. The equivalent inductance matching structure has dimensions of 20 μm × 200 μm, and the equivalent capacitance matching structure is 200 μm × 80 μm. The simulation results of the TL structure are shown in Figure 4: in the frequency band of 0–40 GHz, the reflection coefficient (S11) is less than -20 dB, and the transmission loss (S21) is less than 0.55 dB, demonstrating excellent RF performance.



（a） （b） （c） （d）

**Figure 3** (a) Schematic of a Typical TL Structure; (b) TSV Coaxial-Like Structure; (c) Transition Structure—Microstrip Line; (d) Transition Structure—Stripline

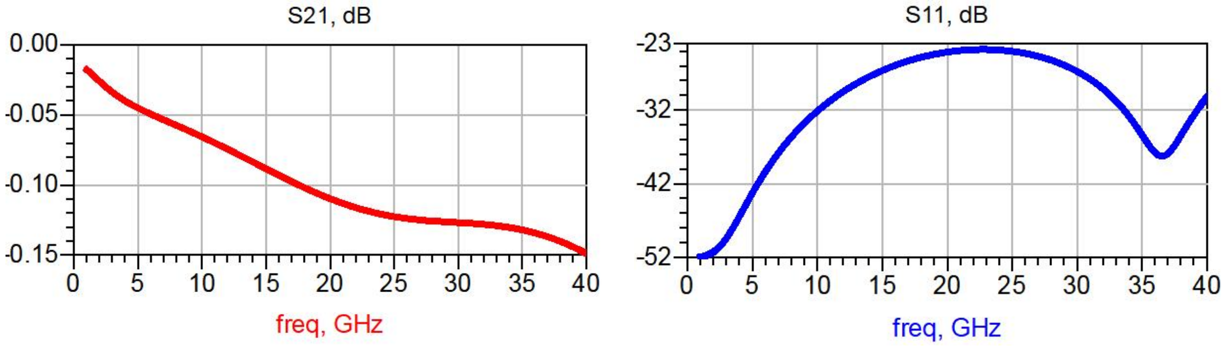


**Figure 4** Simulated S-Parameters of the TL Structure: (a) S11; (b) S21

Upon completion of the layout design, the overall configuration of the microsystem is illustrated in Figure 5. Figure 5(a) and 5(b) show the chip-layer layouts of the upper and lower sub-modules, respectively; Figure 5(c) presents the complete 3D structure of the microsystem; and Figure 5(d) displays an exploded view of each structural layer, clearly illustrating the hierarchical assembly architecture.

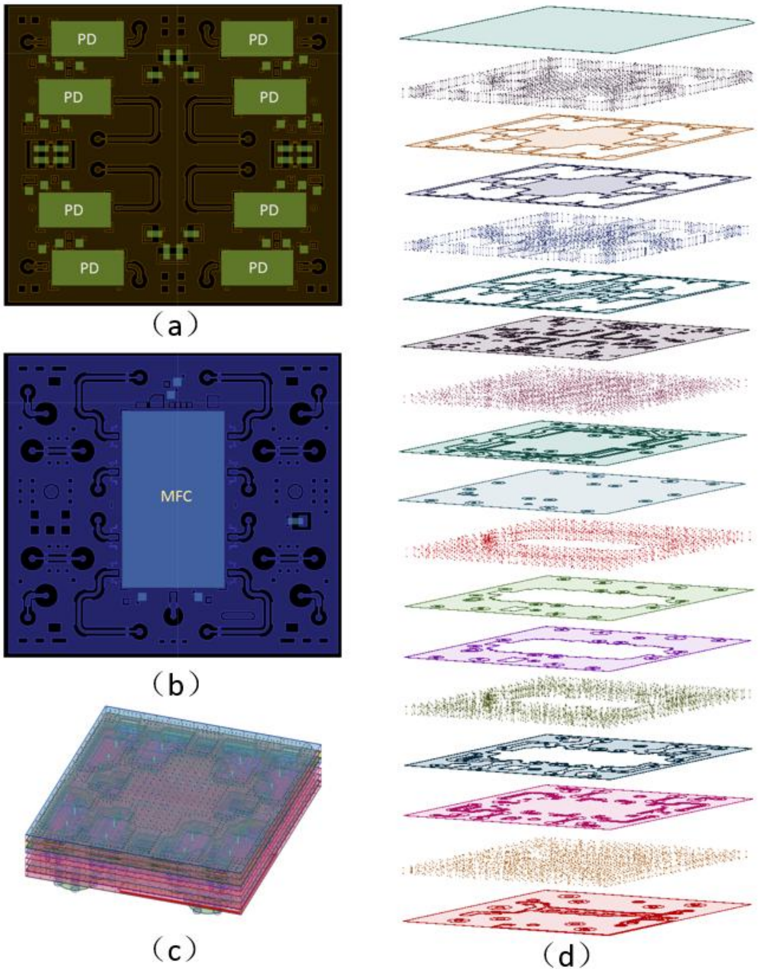


**Figure 5** (a) Chip Layout of the Upper Sub-Module; (b) Chip Layout of the Upper Sub-Module; (c) Complete 3D Structure of the Microsystem; (d) Exploded View of Each Layer

## 3 FABRICATION PROCESS

As noted earlier, the 8-channel transmit microsystem reported in this paper is constructed by stacking two sub-modules, and each sub-module is fabricated via wafer-level packaging of an upper silicon interposer (U), a middle silicon interposer (M), and a bottom silicon interposer (B) (as shown in Figure 6). This section details the fabrication processes of these three silicon interposers and the subsequent microassembly process of the sub-modules.

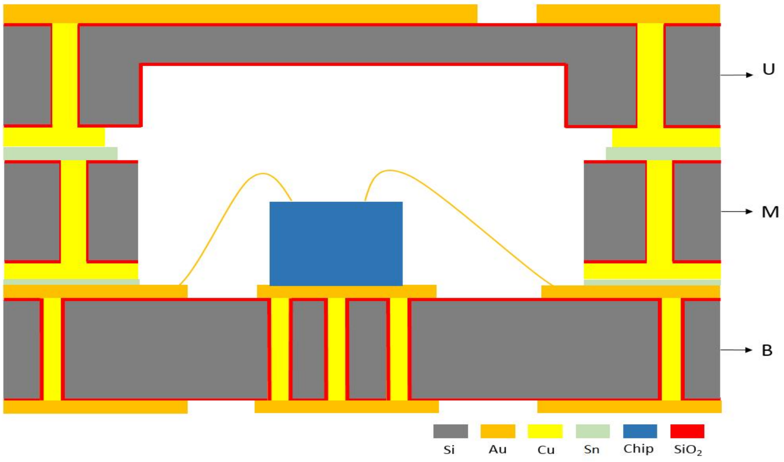


**Figure 6** Wafer-Level Packaging of a Single-Layer Sub-Module

### 3.1 Fabrication of the Bottom Silicon Interposer (B)

The structural configuration of the bottom silicon interposer (B) is shown in Figure 7, with a nominal thickness of 200 μm.

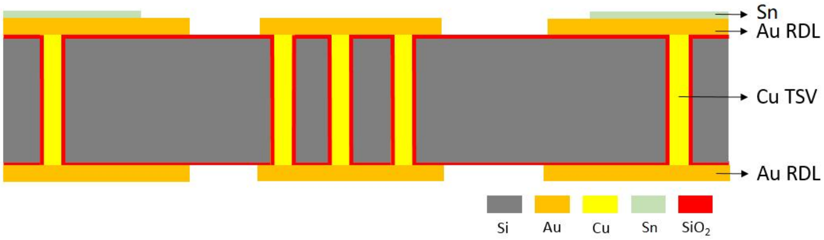


**Figure 7** Structure of the Bottom Silicon Interposer (B)

The fabrication of the bottom silicon interposer commences with TSV etching, followed by the deposition of an insulating layer and a seed layer on the wafer surface via chemical vapor deposition (CVD) and physical vapor deposition (PVD), respectively (as shown in Figure 8(a)). Subsequently, copper electroplating is performed to fill the TSVs (as depicted in Figure 8(b)). Excess metal on the wafer surface is removed by chemical mechanical polishing (CMP) to complete the TSV fabrication (as shown in Figure 8(c)). Next, a redistribution layer (RDL) is patterned on the wafer surface through seed layer deposition, photolithography, and electroplating to realize electrical interconnection between planar patterns and vias (as illustrated in Figure 8(d)). To maximize the process compatibility of the silicon-based microsystem in subsequent assembly processes (primarily for wire bonding and eutectic bonding), the seed layer is retained after stripping the photoresist of the RDL, facilitating the subsequent photolithography and electroplating of Cu and Sn layers. This design not only enables subsequent Cu-Sn bonding but also prevents oxidation of the electroplated copper layer during wire bonding. The fabrication of the electroplated Sn layer marks the completion of the front-side structure of the bottom silicon interposer (as shown in Figure 8(e)). The back-side fabrication process of the bottom silicon interposer initiates with temporary bonding (as depicted in Figure 8(f)), where the completed front-side structure is protected by a temporary bonding wafer. The copper layer at the bottom of the TSVs is fully exposed via grinding and CMP (as shown in Figure 8(g)). An RDL is then formed on the back surface through seed layer deposition, photolithography, and electroplating (as illustrated in Figure 8(h)). Finally, photoresist is spin-coated on the RDL to form a solder mask layer. After removing the temporary bonding wafer, the final structural configuration of the bottom silicon interposer is obtained (as shown in Figure 8(i)).

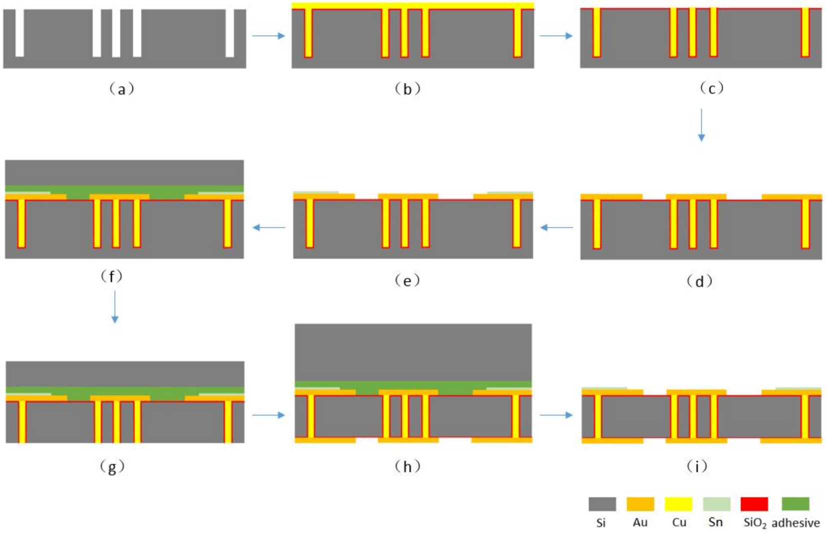


**Figure 8** Fabrication Process of the Bottom Silicon Interposer (B)

### 3.2 Fabrication of the Middle Silicon Interposer (M)

The structure of the middle silicon interposer (M) is presented in Figure 9, which features a hollowed-out design with a thickness of 250 μm to avoid the regions designated for chip mounting and wire bonding. Similar to the bottom interposer (B), the surface metal layer of the middle interposer (M) is also pre-tinned to enable subsequent bonding.

**Figure 9** Structure of the Middle Silicon Interposer (M)

Considering manufacturing process compatibility, the middle silicon interposer is fabricated starting from the back side of the wafer. First, TSVs with a diameter of 30 μm and a depth of 250 μm (φ30 × 250 μm) are etched, followed by the deposition of an insulating layer and a seed layer on the wafer via CVD and PVD, respectively (as shown in Figure 10(a)). Copper electroplating is then performed to fill the TSVs (as depicted in Figure 10(b)). Excess metal is removed by CMP to complete the TSV fabrication (as shown in Figure 10(c)). An RDL is subsequently patterned on the back surface through seed layer deposition, photolithography, and electroplating to achieve electrical interconnection between planar patterns and vias (as illustrated in Figure 10(d)). A temporary bonding process is then employed to protect the back surface of the wafer, while the front-side fabrication process is initiated (as shown in Figure 10(e)). The copper at the bottom of the TSVs is fully exposed via grinding and CMP (as depicted in Figure 10(f)). The RDL and electroplated Sn layer are then fabricated on the front surface through seed layer deposition, photolithography, and electroplating (as shown in Figure 10(g)). Finally, dry etching is performed to form the hollowed-out structure of the middle silicon interposer (as illustrated in Figure 10(h)). After removing the temporary bonding wafer, the final structure of the middle silicon interposer is obtained (as shown in Figure 10(i)).

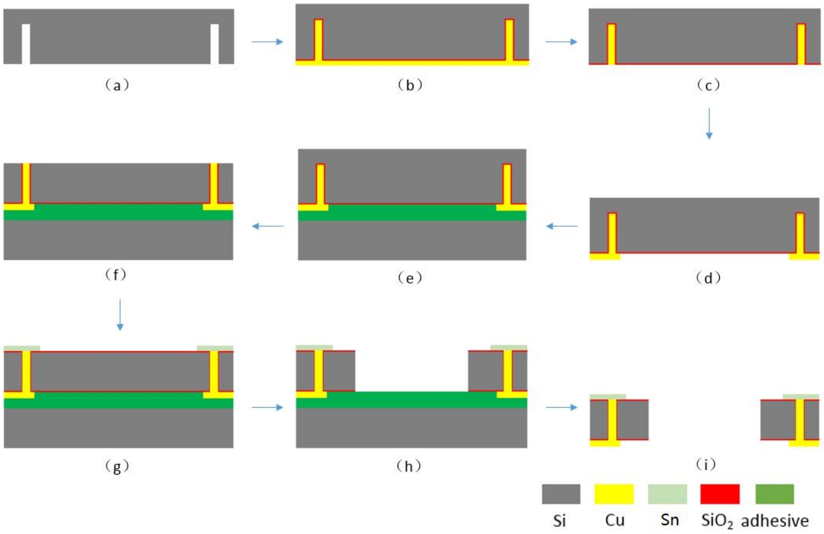


**Figure 10** Fabrication Process of the Middle Silicon Interposer (M)

### 3.3 Fabrication of the Upper Silicon Interposer (U)

The structural configuration of the upper silicon interposer (U) is shown in Figure 11, with a thickness of 250 μm. A deep cavity with a depth of 50 μm is fabricated on the upper interposer (U) to avoid the areas for chip mounting and wire bonding, ensuring sufficient spatial clearance for component assembly.

**Figure 11** Structure of the Upper Silicon Interposer (U)

The fabrication of the upper silicon interposer also begins with the etching of TSVs (φ30 × 250 μm), followed by the deposition of an insulating layer and a seed layer on the wafer via CVD and PVD, respectively (as shown in Figure 11(a)). Copper electroplating is then carried out to fill the TSVs (as depicted in Figure 11(b)), and excess metal is removed by CMP to complete the TSV fabrication (as shown in Figure 11(c)). An RDL is subsequently patterned on the wafer surface through seed layer deposition, photolithography, and electroplating to realize electrical interconnection between planar patterns and vias (as illustrated in Figure 11(d)). A temporary bonding process is then introduced to protect the front surface of the wafer, while the back-side fabrication process is initiated (as shown in Figure 11(e)). The copper at the bottom of the TSVs is fully exposed via grinding and CMP (as depicted in Figure 11(f)). Dry etching is then performed to fabricate a 50 μm-deep cavity on the upper silicon interposer (as shown in Figure 11(g)). Finally, copper metallization is formed on the wafer surface through a series of processes including CVD for insulating layer deposition, PVD for seed layer deposition, photolithography, and electroplating (as illustrated in Figure 11(h)). After removing the temporary bonding wafer, the final structural configuration of the upper silicon interposer is obtained (as shown in Figure 11(i)).

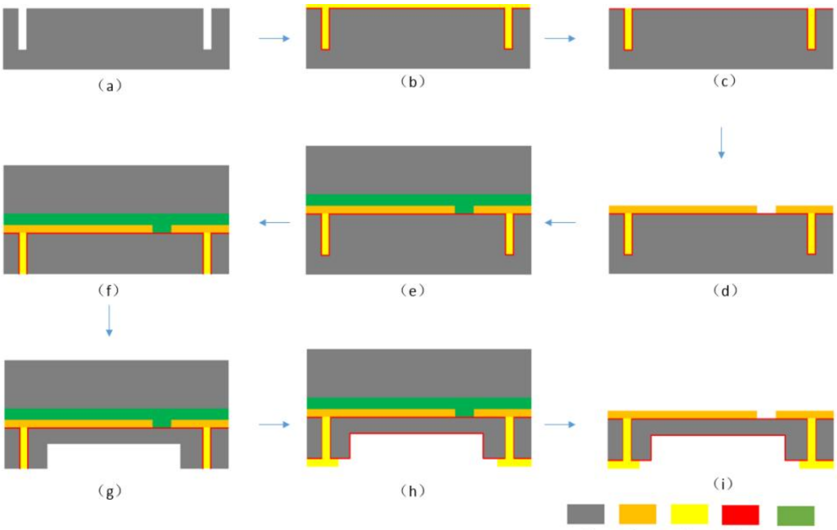
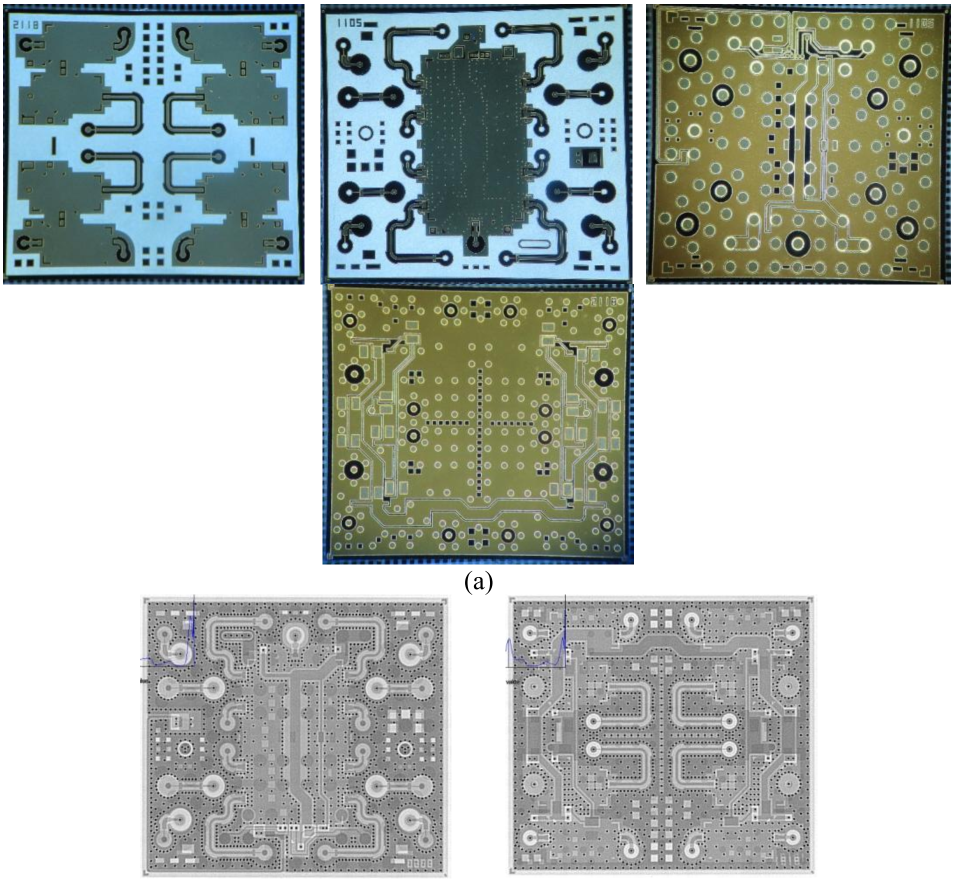


**Figure 11** Fabrication Process of the Upper Silicon Interposer (U)

### 3.4 Characterization of the Silicon Interposers

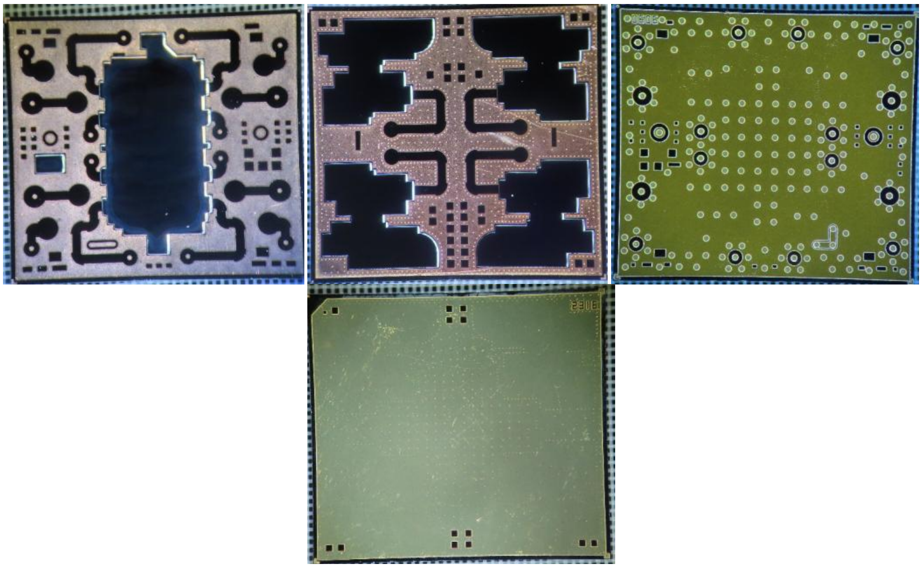
The optical photograph and X-ray image of the bottom silicon interposer are presented in Figure 12, respectively. The scanning electron microscopy (SEM) images and X-ray images of the middle and upper silicon interposers are shown in Figure 13, respectively, verifying the structural integrity and fabrication quality of the interposers.



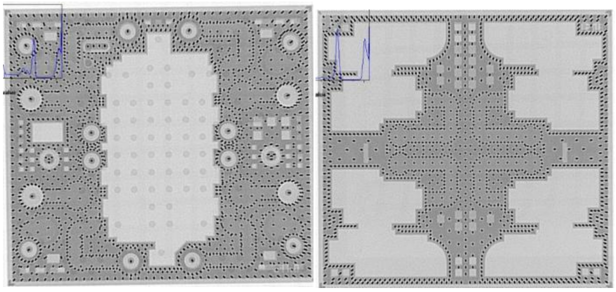
(a)

(b)

**Figure 12** (a) Photograph of the Bottom Silicon Interposer; (b) X-ray Image of the Bottom Silicon Interposer



(a)



(b)

**Figure 13** (a) SEM Images of the Middle and Top Silicon Interposers; (b) X-Ray Images of the Middle And Top Silicon Interposers

### 3.5 Three-Layer Cu-Sn Eutectic Bonding and Differentiated Temperature Gradient Soldering

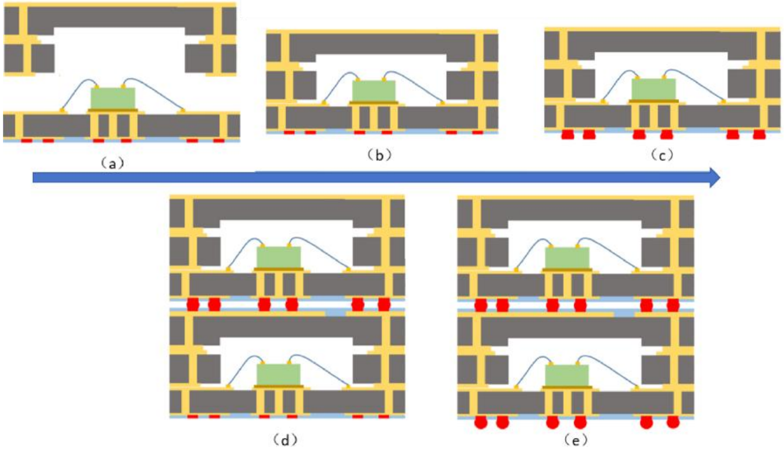
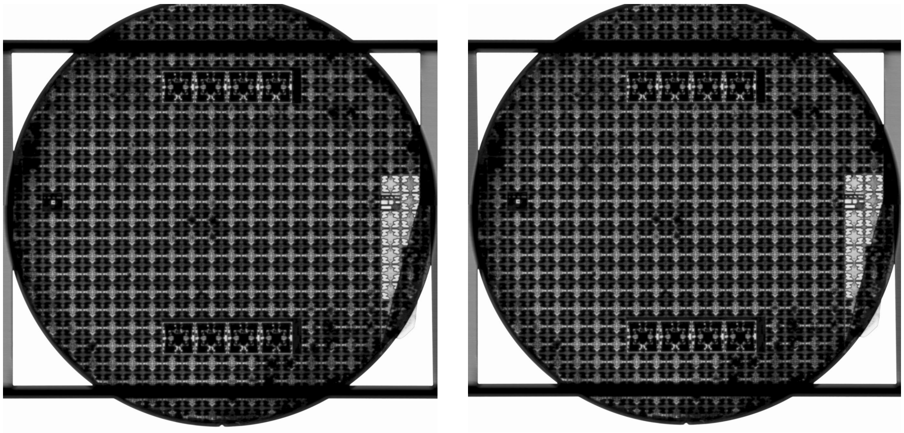


**Figure 14** Microassembly Process of the Microsystem

Subsequent to the fabrication of the interposer wafers, the microassembly process of the microsystem is carried out as follows. First, chip mounting and wire bonding are completed on the bottom interposer (B) wafer (as shown in Figure 14(a)). Then, chip-level bonding is performed between the bottom interposer (B) wafer and the combined MU interposer wafer (the middle (M) and upper (U) interposer wafers are pre-bonded at the wafer level and then diced) (as depicted in Figure 14(b)). The bonded wafer is then diced to form individual modular units. SAC305 solder paste is printed on the bottom of the upper sub-module, Pb90Sn10 high-lead solder balls are placed, and reflow ball mounting is performed at 210 °C–230 °C (as shown in Figure 14(c)). Next, SAC305 solder paste is printed on the top of the lower sub-module, and the stacking of the two sub-modules is completed via reflow soldering at 210 °C–230 °C (as illustrated in Figure 16(d)). Finally, Sn63Pb37 solder paste is printed on the bottom of the lower sub-module, Pb90Sn10 high-lead solder balls are placed, and reflow ball mounting is conducted at 180 °C–200 °C (as shown in Figure 14(e)). At this stage, the microassembly process is completed, and the final 8-channel transmit microsystem is formed.

It should be noted that the aforementioned wafer-level bonding is realized based on Cu-Sn plating layers. The material system adopted for wafer-level bonding in this work is Cu-Sn with a bonding temperature of 280 °C. The structural configurations of the interposers after two-layer and three-layer bonding, along with the scanning acoustic microscopy (C-SAM) images of the bonding regions, are presented in Figure 15, which demonstrate the excellent bonding quality with no obvious defects. To verify the sufficient interdiffusion and reaction between Cu and Sn in the bonding region, SEM imaging, focused ion beam (FIB) slicing, and energy dispersive X-ray (EDX) composition analysis are performed on the bonded samples. The SEM image of the sample is shown in Figure 16(a); the marked regions in the bonding area (as depicted in Figure 16(b)) are selected for FIB milling, and the measurement points for EDX composition analysis are marked (as shown in Figure 16(c)). According to the EDX composition analysis results (as illustrated in Figure 16(d)), the atomic ratio of Cu to Sn in the Cu-Sn bonding region is greater than 3:1, indicating the formation of stable intermetallic compounds within the range of ε phase ($Cu_3Sn$) and α phase ($Cu_9Sn$~Cu) [22]. Cu-Sn intermetallic compounds offer two key advantages: (1) High compactness: The dense microstructure of

Cu-Sn intermetallic compounds provides a reliable basis for hermetic packaging. Under the fine leak detection test condition (helium mass spectrometer) at 5 atmospheres, the helium leakage rate of each sub-module is lower than $2\times10^{-9}$ Pa·m³/s, which fully meets the hermetic packaging requirements specified in the GJB military standards. (2) High melting point: The melting point of Cu-Sn intermetallic compounds exceeds 650 °C, rendering them essentially unaffected by subsequent manufacturing processes with a typical temperature range of 100 °C–400 °C [23-25].



(a) (b)

**Figure 15** (a) C-SAM Image of the Wafer after M+U+B1 Bonding; (b) C-SAM Image after M+U+B2 Bonding

Another critical consideration is the adoption of two types of solder paste with distinct reflow temperatures in the microassembly process: SAC305 solder paste with a reflow temperature of 210 °C–230 °C and Sn63Pb37 solder paste with a reflow temperature of 180 °C–200 °C. The reflow temperature ranges of these two solder pastes exhibit almost no overlap, which effectively avoids the risk of secondary melting of the solder paste during the sequential assembly process and provides a reliable technical solution for modular stacking.

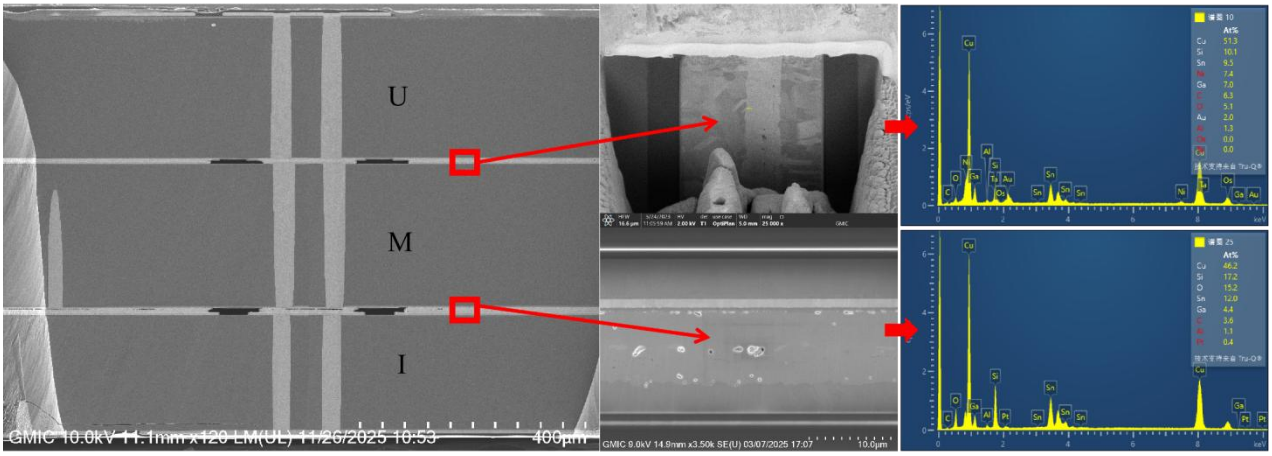
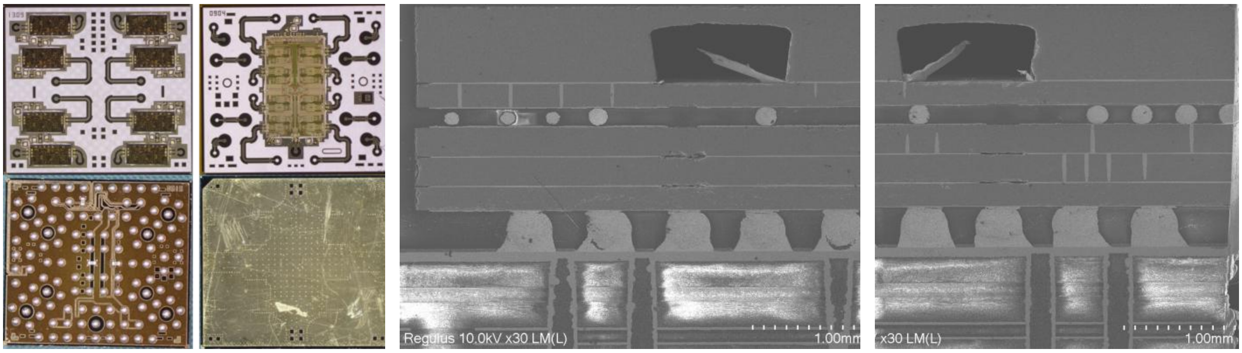


**Figure 16** (a) SEM Image of the Sample; (b) Marked Region for Ion Milling; (c) Ion Milling Position and EDX Analysis Points; (d) EDX Composition Analysis Results

## 4 CHARACTERIZATION AND ELECTRICAL PERFORMANCE MEASUREMENT

### 4.1 Microsystem Morphological Characterization

Figure 17 shows the internal optical photographs of the 8-channel transmit microsystem and the overall SEM cross-sectional image. The internal photograph of the upper sub-module (power amplifier, PA) is presented in Figure 17(a), the internal photograph of the lower sub-module (amplitude-phase multifunctional chip, MFC) is shown in Figure 17(b), and the SEM cross-sectional image of the entire microsystem is depicted in Figure 17(c), clearly revealing the hierarchical stacking structure and the integrity of the internal assembly.



(a) (b) (c)

**Figure 19** (a) Internal Photograph of the Upper Sub-Module (PA); (b) Internal Photograph of the Lower Sub-Module (MFC); (c) SEM Image of the Entire Microsystem

### 4.2 Microsystem Electrical Performance Measurement

After power-on testing, the single-channel output power of the module is measured to be greater than 23 dBm (the insertion loss introduced by the test board and connecting cables has been de-embedded for accurate performance evaluation), as shown in Figure 18. The in-band gain of the transmit channel reaches up to 23 dB (as presented in Figure 19). Supported by the amplitude-phase multifunctional chip (MFC), the microsystem achieves 6-bit phase shifting, and the root mean square (RMS) value of the in-band phase shift accuracy is illustrated in Figure 20, demonstrating excellent phase control performance.

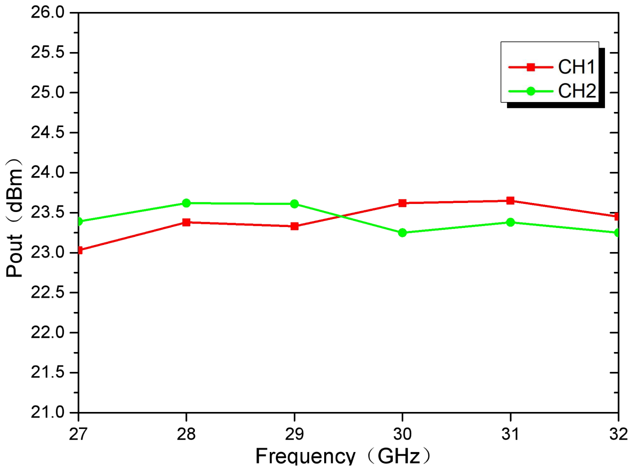


**Figure 18** Channel Output Power

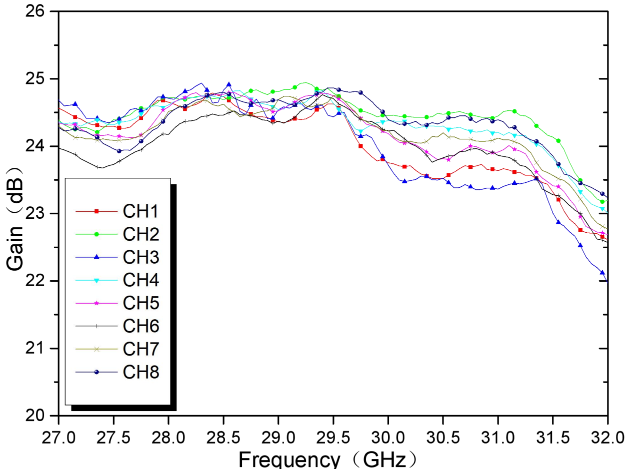


**Figure 19** In-Band Gain Curves of 8 Channels

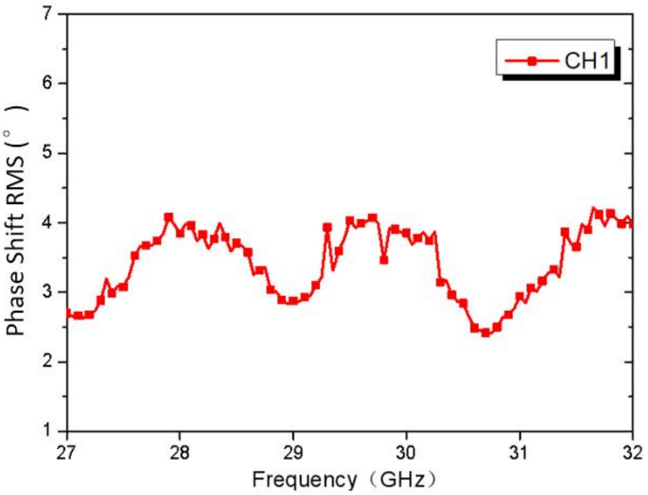


**Figure 20** RMS Value of in-Band Phase Shift Accuracy

## 5 CONCLUSION

Based on silicon-based 3D heterogeneous integrated microsystem technology, this paper successfully fabricates a high-performance Ka-band 8-channel transmit microsytem with an operating frequency band over 27–32 GHz, a saturated output power of 23 dBm, an overall dimensions of 9.1 mm × 8.5 mm × 3.25 mm, and a weight of less than 0.1 g per channel. By introducing capacitive and inductive transition structures in the 3D passive interconnections of the microsystem, up to 40GHz broadband impedance matching is realized. Two key innovative technologies are proposed and validated: the Cu-Sn bonding technology with a pre-tinned Sn layer and the modular stacking technology based on differentiated temperature gradient soldering. These technologies effectively address the process compatibility issues encountered during module assembly and overcome the high-temperature and high-cost limitations of traditional Au-based hermetic packaging systems. The electrical performance of the fabricated microsystem is comprehensively evaluated, and the measured results show excellent agreement with the design specifications and simulation results, verifying the feasibility and effectiveness of the proposed design and fabrication scheme.

The proposed silicon-based 3D heterogeneous integration scheme and key manufacturing technologies provide a viable technical approach for the high-density, high-performance, and high-frequency integration of phased array TR modules, and also lay a solid foundation for the further development and practical application of silicon-based 3D heterogeneous microsystems in the field of millimeter-wave phased array radars.

## COMPETING INTERESTS

The authors have no relevant financial or non-financial interests to disclose.

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